RECEIVED
CENTRAL FAX CENTER

FEB 2 0 2007

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Torsten Partsch	Examiner:	Michael B. McFadden
Serial No.:	10/706,438	Group Art Unit:	2188
Filed:	November 12, 2003	Docket No.:	I331.102.101/2003P52601US
Title:	RANDOM ACCESS MEMORY WITH OPTIONAL COLUMN ADDRESS STROBE LATENCY OF ONE		

CERTIFICATE OF TRANSMISSION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

I hereby certify that the following paper(s) are being facsimile transmitted to the U.S. Patent and Trademark Office, Fax. No. (571) 273-8300 on the date shown below:

1. Transmittal Sheet containing Certificate of Transmission (1 pg.);
2. Appeal Brief Under 37 C.F.R. 41.37 (31 pgs.).

Date: February 20, 2007

By: Mark Peterson

MAP:kmh

Name: Mark A. Peterson (Reg. No. 50,485)

33 Pages (including cover page)

RECEIVED
CENTRAL FAX CENTER
FEB 20 2007

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Torsten Partsch	Examiner:	Michael B. McFadden
Serial No.:	10/706,438	Group Art Unit:	2188
Filed:	November 12, 2003	Docket:	I331.102.101/2003P52601US
Due Date:	February 20, 2007		
Title:	**RANDOM ACCESS MEMORY WITH OPTIONAL COLUMN ADDRESS STROBE LATENCY OF ONE**		

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir

We are transmitting herewith the attached:

- ☒ Certificate of Transmission (1 pg.).
- ☒ Transmittal Sheet containing Certificate of Transmission (1 pg.).
- ☒ Appeal Brief to the Board of Patent Appeals and Interferences of the U.S. Patent and Trademark Office (31 pgs.).
- ☒ The Commissioner is authorized to charge $500.00 to deposit account no. 500471 to cover the Appeal Brief fee.

Please consider this a PETITION FOR EXTENSION OF TIME for a sufficient number of months to enter these papers, if appropriate. At any time during the pendency of this application, please charge any additional fees or credit overpayment to Deposit Account No. 500471.

Customer No. 025281

By: Mark Peterson
Name: Mark A. Peterson
Reg. No.: 50,485

CERTIFICATE UNDER 37 C.F.R. 1.8:

The undersigned hereby certifies that this paper or papers, as described herein, are being transmitted via facsimile to Facsimile No. (571) 273-8300 on this 20th day of February, 2007.

By: Mark Peterson
Name: **Mark A. Peterson**

RECEIVED
CENTRAL FAX CENTER

FEB 2 0 2007

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant:	Torsten Partsch	Examiner: Michael B. McFadden
Serial No.:	10/706,438	Group Art Unit: 2188
Filed:	November 12, 2003	Docket: I331.102.101/2003P52601US
Due Date:	February 20, 2007	
Title:	RANDOM ACCESS MEMORY WITH OPTIONAL COLUMN ADDRESS STROBE LATENCY OF ONE	

APPEAL BRIEF UNDER 37 C.F.R. § 41.37

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This Appeal Brief is submitted in support of the Notice of Appeal filed on December 20, 2006, appealing the final rejection of claims 1-38 of the above-identified application as set forth in the Final Office Action mailed September 20, 2006.

The U.S. Patent and Trademark Office is hereby authorized to charge Deposit Account No. 50-0471 in the amount of $500.00 for filing a Brief in Support of an Appeal as set forth under 37 C.F.R. § 41.20(b)(2). At any time during the pendency of this application, please charge any required fees or credit any overpayment to Deposit Account No. 50-0471.

Appellant respectfully requests consideration and reversal of the Examiner's rejection of pending claims 1-38.

Appeal Brief to the Board of Patent Appeals and Interferences
Applicant: Torsten Partsch
Serial No.: 10/706,438
Filed: November 12, 2003
Docket No.: I331.102.101/2003P52601US
Title: RANDOM ACCESS MEMORY WITH OPTIONAL COLUMN ADDRESS STROBE LATENCY OF ONE

TABLE OF CONTENTS

REAL PARTY IN INTEREST

The intellectual property embodied in the pending application is assigned to Infineon Technologies North America Corp.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant that will have a bearing on the Board's decision in the present Appeal.

STATUS OF CLAIMS

In a Final Office Action mailed September 20, 2006, claims 1-38 were finally rejected. Claims 1-38 are pending in the application. Claims 1-38 are the subject of the present Appeal.

STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Office Action mailed September 20, 2006.

SUMMARY OF THE CLAIMED SUBJECT MATTER

The subject matter of the independent claims involved in the Appeal is related to a random access memory.

One aspect of the present invention, as claimed in independent claim 1, provides a random access memory (10). The random access memory (10) includes an array of memory cells (32) and a memory (116a-116d) configured to receive data from the array of memory cells (32). The random access memory (10) includes a bypass circuit (114) configured to receive the data from the array of memory cells (32) and to bypass the memory (116a-116d). The random access memory (10) includes a circuit (118, 112, 113, 150, 156) configured to select between receiving the data from the memory (116a-116d) to provide first output signals and receiving the data from the bypass circuit (114) to provide second output signals based on a column address strobe latency select signal. *See Specification*, at page 3, line 1 through line 32; page 6, line 18 through page 9, line 19; and Figures 1, 3, and 4.

Another aspect of the present invention, as claimed in dependent claim 8, provides a random access memory (10). The random access memory (10) includes an array of memory cells (32) and a memory (116a-116d) configured to receive data from the array of memory cells (32). The random access memory (10) includes a bypass circuit (114) configured to receive the data from the array of memory cells (32) and to bypass the memory (116a-116d). The random access memory (10) includes a circuit (118, 112, 113, 150, 156) configured to select between receiving the data from the memory (116a-116d) to provide first output signals and receiving the data from the bypass circuit (114) to provide second output signals based on a column address strobe latency select signal. The circuit (118, 112, 113, 150, 156) includes a first circuit (118) configured to receive first rise and fall signals to serialize the data from the memory (116a-116d). The circuit (118, 112, 113, 150, 156) includes a second circuit (150) configured to receive second rise and fall signals to serialize the data from the bypass circuit (114). The circuit (118, 112, 113, 150, 156) includes a multiplexer (156) configured to select between serialized data from the first circuit (118) and serialized data from the second circuit (150) based on the column address strobe latency select signal. *See Specification*, at page 3, line 1 through line 32; page 6, line 18 through page 9, line 19; and Figures 1, 3, and 4.

Yet another aspect of the present invention, as claimed in independent claim 17, provides a random access memory (10). Random access memory (10) includes a first in/first out memory (116a-116d) and a bypass circuit (114) that bypasses the first in/first out memory (116a-116d). The random access memory (10) includes a control circuit (112, 113) configured to provide first signals and second signals, wherein the first signals latch data from the first in/first out memory (116a-116d) to provide a column address strobe latency of greater than one and the second signals latch data from the bypass circuit (114) to provide a column address strobe latency of one. *See Specification*, at page 3, line 1 through line 32; page 6, line 18 through page 9, line 19; and Figures 1, 3, and 4.

Yet another aspect of the present invention, as claimed in independent claim 25, provides a random access memory (10). The random access memory (10) includes a memory circuit (116a-116d) and a bypass circuit (114) configured to bypass the memory circuit (116a-116d). The random access memory (10) includes a first rise/fall circuit (118) configured to receive data from the memory circuit (116a-116d) to provide a first output

signal and a second rise/fall circuit (150) configured to receive data from the bypass circuit (114) to provide a second output signal. The random access memory (10) includes a multiplexer (156) configured to select between the first output signal and the second output signal based on a column address strobe latency select signal. *See Specification*, at page 3, line 1 through line 32; page 6, line 18 through page 9, line 19; and Figures 1, 3, and 4.

Yet another aspect of the present invention, as claimed in independent claim 31, provides a random access memory (10). The random access memory (10) includes means (116a-116d) for storing data read from an array of memory cells (32) and means (114) for receiving the data read from the array of memory cells (32) to bypass the means (116a-116d) for storing data. The random access memory (10) includes means (118, 112, 113, 150, 156) for retrieving the data from the means (116a-116d) for storing the data if column address strobe latency is greater than one and means (118, 112, 113, 150, 156) for retrieving the data from the means (114) for receiving the data if the column address strobe latency is one. *See Specification*, at page 3, line 1 through line 32; page 6, line 18 through page 9, line 19; and Figures 1, 3, and 4.

Yet another aspect of the present invention, as claimed in independent claim 34, provides a method for reading data from a random access memory (10) in a column address strobe latency of one. The method includes initiating a read command on a first edge of a clock cycle, receiving data read from the array of memory cells (10) in a bypass circuit (114) during the clock cycle, and retrieving the data from the bypass circuit (114) during the clock cycle. *See Specification*, at page 3, line 1 through line 32; page 6, line 18 through page 9, line 19; and Figures 1, 3, and 4.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

I. Whether claims 1-3 and 31 are patentable under 35 U.S.C. § 102(b) over Usami, U.S. Patent No. 6,205,516 (Usami) and whether claims 4-7, 9-16, 32, and 33 are patentable under 35 U.S.C. § 103(a) over Usami.

II. Whether claim 8 is patentable under 35 U.S.C. § 103(a) over Usami.

III. Whether claims 17 and 18 are patentable under 35 U.S.C. § 102(b) over Usami and whether claims 19-24 are patentable under 35 U.S.C. § 103(a) over Usami.

IV. Whether claims 25-30 are patentable under 35 U.S.C. § 103(a) over Usami.

V. Whether claims 34-38 are patentable under 35 U.S.C. § 103(a) over Usami.

ARGUMENT

I. The Applicable Law

With regard to a 35 U.S.C. § 102(b) anticipation rejection: "A person shall be entitled to a patent unless- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States." 35 U.S.C. § 102(b).

A rejection based on 35 U.S.C. § 102(b) can be overcome by: persuasively arguing that the claims are patentably distinguishable from the prior art; or, amending the claims to patentably distinguish over the prior art. M.P.E.P. § 706.02(b).

With regard to a 35 U.S.C. § 103 obviousness rejection: "Patent examiners carry the responsibility of making sure that the standard of patentability enunciated by the Supreme Court and by the Congress is applied in each and every case." M.P.E.P. 2141 (emphasis in the original). The Examiner bears the burden under 35 U.S.C. § 103 in establishing a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

Three criteria must be satisfied to establish a *prima facie* case of obviousness. First, the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would teach, suggest, or motivate one to modify a reference or to combine the teachings of multiple references. *In re Fine* at 1074. Second, the prior art can be modified or combined only so long as there is a reasonable expectation of success. *In re Merck & Co., Inc.*, 800 F.2d 1091, 231 USPQ 375, 379 (Fed. Cir. 1986). Third, the reference or combined references must teach or suggest all of the claim limitations. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (C.C.P.A. 1974).

The court in *Fine* stated:

> Obviousness is tested by "what the combined teaching of the references would have suggested to those of ordinary skill in the art." But it "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination."

> And "teachings of references can be combined *only* if there is some suggestion or incentive to do so."

In re Fine, 5 USPQ2d at 1599 (citations omitted).

There must be some teaching somewhere that provides the suggestion or motivation to combine prior art teachings and applies that combination to solve the same or similar problem that it addresses. *In re Nilssen*, 851 F.2d 1401, 1403, 7 USPQ2d 1500, 1502 (Fed. Cir. 1988); *In re Wood*, 599 F.2d 1032, 1037, 202 USPQ 171, 174 (C.C.P.A. 1979). In particular, "The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based upon applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142 (emphasis added).

The test for obviousness under § 103 must take into consideration the invention as a whole; that is, one must consider the particular problem solved by the combination of elements that define the invention. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 USPQ 543, 551 (Fed. Cir. 1985). Furthermore, claims must be interpreted in light of the specification, claim language, other claims, and prosecution history. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1568, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987), *cert. denied*, 481 U.S. 1052 (1987). At the same time, a prior patent cited as a § 103 reference must be considered in its entirety, "*i.e.* as a *whole*, including portions that lead away from the invention." *Id.* That is, the Examiner must recognize and consider not only the similarities, but also the critical differences between the claimed invention and the prior art as one of the factual inquiries pertinent to any obviousness inquiry under 35 U.S.C. § 103. *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990) (emphasis added). Finally, the Examiner must avoid hindsight. *Id.*

With regard for the test for obviousness under § 103, a statement that modifications of the prior art to meet the claimed invention would have been " 'well within the ordinary skill of the art at the time the claimed invention was made' " because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the teachings of the references. *Ex parte Levengood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993); M.P.E.P. § 2143.01 (emphasis in the original).

In conclusion, an applicant is entitled to a patent grant if any one of the elements of a prima facie case of obviousness is not established. The Federal Circuit has endorsed this view in stating: "If examination at the initial stage does not produce a prima facie case of unpatentability, then without more the applicant is entitled to grant of the patent." In re Oetiker, 977 F.2d 1443, 1446, 24 USPQ2d 1443, 1448 (Fed. Cir. 1992).

II. Rejection of claims 1-3 and 31 under 35 U.S.C. § 102(b) as being unpatentable over Usami U.S. Patent No. 6,205,516 (Usami) and rejection of claims 4-7, 9-16, 32, and 33 under 35 U.S.C. § 103(a) as being unpatentable over Usami.

Independent claims 1 and 31 are patentably distinct from Usami.

Appellant submits that Usami fails to teach or suggest the invention recited by independent claim 1 including **a bypass circuit configured to receive the data from the array of memory cells and to bypass the memory; and a circuit configured to select between receiving the data from the memory to provide first output signals and receiving the data from the bypass circuit to provide second output signals based on a column address strobe latency select signal.**

Usami discloses that each SDRAM includes a DRAM core 37. The DRAM core 37 is constructed from a plurality of banks. The SDRAM further includes a clock buffer 30, a command decoder 31, an address buffer/register and bank select 32, a pair of control signal latches 34, a mode register 35, a pair of column address counters 36, and an I/O data buffer/register 33. (Col. 7, line 64 - col. 8, line 3). The I/O data buffer/register 33 serves as a buffer circuit or register circuit for temporarily storing data to be written to the DRAM core 37 or for temporarily storing data read from the DRAM core 37. The I/O data buffer/register 33 is connected to the corresponding data bus "I/O data DQ0-DQ3" that is connected to the CPU 1. (Col. 9, lines 62 - col. 10, line 1).

The Examiner submits "SDRAM is inherently created from a memory array, a memory configured to receive data from the array, a bypass circuit, and a circuit that will select the programmed mode. Figure 4 shows that depending on the contents of the CAS Latency bits A4, A5, and A6 the CL (CAS latency) will vary accordingly as described in Claims 2 and 3." (Final Office Action mailed September 20, 2006, page 3). The Examiner also submits in the Response to Arguments "Usami teaches varying CAS Latencies (CLs).

Cache Latencies are varied by changing the number of pipeline stages in the cache. A CL of one means that a cache has one pipeline stage, a CL of two means two pipeline stages, and so on. Therefore, in providing multiple CLs Usami inherently teaches bypassing one or more pipeline stages based on setting of the CAS Latency bits. In bypassing a pipeline stage, a bypass circuit and a circuit configured to select between receiving data are inherent." (Final Office Action mailed September 20, 2006, pages 5-6).

Appellant submits that it is not inherent in Usami that a bypass circuit is used as recited in claim 1. As the Federal Circuit has stated, "[i]nherent anticipation requires that the missing descriptive material is 'necessarily present,' not merely probably or possibly present, in the prior art." *Trintec Indus., v. Top-U.S.A. Corp.*, 63 USPQ2d 1597, 1599 (Fed. Cir. 2002) (quoting *In re Robertson*, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)). Since varying the CAS latency in Usami could be performed without utilizing a bypass circuit as recited in claim 1, the limitations of claim 1 are not inherent in Usami as submitted by the Examiner. In addition, there is not a single reference to a cache memory including pipeline stages in Usami.

Figures 2 and 4 and the associated text of Usami do not disclose a bypass circuit or a circuit configured to select between receiving the data from the memory array to provide first output signals and receiving the data from the bypass circuit to provide second output signals based on a column address strobe latency select signal as recited in independent claim 1. In contrast, Usami merely discloses an I/O data buffer/register 33 for receiving data from the DRAM core 37 or writing data to the DRAM core 37. Nowhere in the text or figures does Usami disclose a bypass circuit for routing the data around I/O data buffer/register 33 based on a column address strobe latency select signal. There is also no teaching or suggestion that I/O data buffer/register 33 includes pipeline stages. Even if I/O data buffer/register 33 did include pipeline stages, I/O data buffer/register 33 does not receive a CAS latency select signal for selecting a pipeline stage. The CAS latency select signal is only provided to column address counter 36.

The mode register 35 is for extracting operation mode information, such as the CAS latency, the burst type, and the burst length, from the address data A0-A11 when the mode register 35 receives the address data A0-A11 in correspondence with a predetermined "mode register set" command that is received from the command decoder 31. Mode register 35

supplies each column address counter 36 with a control signal designating the burst length, the burst type, and the CAS latency, thereby controlling count up timing and count up number of the column address counter 36. (Col. 9, lines 45-62). Therefore, Usami discloses controlling the CAS latency based on controlling the column address counter 36, not by using a bypass circuit as recited in claim 1.

In view of the above, Appellant respectfully requests reversal of the rejection of independent claim 1 under 35 U.S.C. § 102(b). Dependent claims 2-7 and 9-16 further define patentably distinct independent claim 1. Accordingly, Appellant believes these dependent claims are also allowable over the cited reference. Appellant respectfully requests reversal of the rejection of claims 2-3 under 35 U.S.C. § 102(b) and the rejection of claims 4-7 and 9-16 under 35 U.S.C. § 103(a).

For the same reasons as discussed above with reference to claim 1, Appellant submits that Usami fails to teach or suggest the invention recited by independent claim 31 including **means for receiving the data read from the array of memory cells to bypass the means for storing data; means for retrieving the data from the means for storing the data if column address strobe latency is greater than one; means for retrieving the data from the means for receiving the data if the column address strobe latency is one.**

In view of the above, Appellant respectfully requests reversal of the rejection of independent claim 31 under 35 U.S.C. § 102(b). Dependent claims 32 and 33 further define patentably distinct independent claim 31. Accordingly, Appellant believes these dependent claims are also allowable over the cited reference. Appellant respectfully requests reversal of the rejection of claims 32 and 33 under 35 U.S.C. § 103(a).

III. Rejection of claim 8 under 35 U.S.C. § 103(a) as being unpatentable over Usami.

Usami fails to render claim 8 *prima facie* obvious.

Appellant submits that Usami fails to teach or suggest the invention recited by dependent claim 8 including **a bypass circuit configured to receive the data from the array of memory cells and to bypass the memory; and a circuit configured to select between receiving the data from the memory to provide first output signals and receiving the data from the bypass circuit to provide second output signals based on a column address strobe latency select signal, wherein the circuit comprises a first circuit**

configured to receive first rise and fall signals to serialize the data from the memory, wherein the circuit comprises a second circuit configured to receive second rise and fall signals to serialize the data from the bypass circuit, and wherein the circuit comprises a multiplexer configured to select between serialized data from the first circuit and serialized data from the second circuit based on the column address strobe latency select signal.

Usami discloses that each SDRAM includes a DRAM core 37. The DRAM core 37 is constructed from a plurality of banks. The SDRAM further includes a clock buffer 30, a command decoder 31, an address buffer/register and bank select 32, a pair of control signal latches 34, a mode register 35, a pair of column address counters 36, and an I/O data buffer/register 33. (Col. 7, line 64 - col. 8, line 3). The I/O data buffer/register 33 serves as a buffer circuit or register circuit for temporarily storing data to be written to the DRAM core 37 or for temporarily storing data read from the DRAM core 37. The I/O data buffer/register 33 is connected to the corresponding data bus "I/O data DQ0-DQ3" that is connected to the CPU 1. (Col. 9, lines 62 - col. 10, line 1).

The Examiner submits "SDRAM is inherently created from a memory array, a memory configured to receive data from the array, a bypass circuit, and a circuit that will select the programmed mode. Figure 4 shows that depending on the contents of the CAS Latency bits A4, A5, and A6 the CL (CAS latency) will vary accordingly as described in Claims 2 and 3." (Final Office Action mailed September 20, 2006, page 3). The Examiner also submits in the Response to Arguments "Usami teaches varying CAS Latencies (CLs). Cache Latencies are varied by changing the number of pipeline stages in the cache. A CL of one means that a cache has one pipeline stage, a CL of two means two pipeline stages, and so on. Therefore, in providing multiple CLs Usami inherently teaches bypassing one or more pipeline stages based on setting of the CAS Latency bits. In bypassing a pipeline stage, a bypass circuit and a circuit configured to select between receiving data are inherent." (Final Office Action mailed September 20, 2006, pages 5-6).

Appellant submits that it is not inherent in Usami that a bypass circuit is used as recited in claim 8. As the Federal Circuit has stated, "[i]nherent anticipation requires that the missing descriptive material is 'necessarily present,' not merely probably or possibly present, in the prior art." *Trintec Indus., v. Top-U.S.A. Corp.*, 63 USPQ2d 1597, 1599 (Fed. Cir.

2002) (quoting *In re Robertson*, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)). Since varying the CAS latency in Usami could be performed without utilizing a bypass circuit as recited in claim 8, the limitations of claim 8 are not inherent in Usami as submitted by the Examiner. In addition, there is not a single reference to a cache memory including pipeline stages in Usami.

Figures 2 and 4 and the associated text of Usami do not disclose a bypass circuit or a circuit configured to select between receiving the data from the memory array to provide first output signals and receiving the data from the bypass circuit to provide second output signals based on a column address strobe latency select signal as recited in claim 8. In contrast, Usami merely discloses an I/O data buffer/register 33 for receiving data from the DRAM core 37 or writing data to the DRAM core 37. Nowhere in the text or figures does Usami disclose a bypass circuit for routing the data around I/O data buffer/register 33 based on a column address strobe latency select signal. There is also no teaching or suggestion that I/O data buffer/register 33 includes pipeline stages. Even if I/O data buffer/register 33 did include pipeline stages, I/O data buffer/register 33 does not receive a CAS latency select signal for selecting a pipeline stage. The CAS latency select signal is only provided to column address counter 36.

The mode register 35 is for extracting operation mode information, such as the CAS latency, the burst type, and the burst length, from the address data A0-A11 when the mode register 35 receives the address data A0-A11 in correspondence with a predetermined "mode register set" command that is received from the command decoder 31. Mode register 35 supplies each column address counter 36 with a control signal designating the burst length, the burst type, and the CAS latency, thereby controlling count up timing and count up number of the column address counter 36. (Col. 9, lines 45-62). Therefore, Usami discloses controlling the CAS latency based on controlling the column address counter 36, not by using a bypass circuit as recited in claim 8.

Further, there is no teaching or suggestion in Usami of a first circuit to serialize the data from the memory and a second circuit to serialize the data from the bypass circuit. In addition, there is no teaching or suggestion in Usami of a multiplexer, let alone a multiplexer configured to select between data from the first circuit and data from the second circuit based on the CAS latency select signal. In contrast, Usami discloses a single circuit, I/O data buffer

register 33, for temporarily storing data to be written to the DRAM core 37 or for temporarily storing data read from the DRAM core 37. (Col. 9, lines 63-66). Regarding these limitations, the Examiner states:

> A programmable SDRAM must inherently contain circuit means for serializing data as initiated by an edge of a clock cycle. The Examiner takes official notice that any combination of clock edges can be combined to provide the instruction to receive data. The motivation for doing so would be to increase system speed for read and write commands. Therefore it would be obvious to use any combination of clock edges to provide the instruction to receive data so that the system can be configured to increase system speed for read and write commands to obtain the invention claimed. (Final Office Action mailed September 20, 2006, page 4).

Usami, however, fails to teach or suggest these claim limitations. In Addition, Appellant submits that a first circuit to serialize the data from the memory, a second circuit to serialize the data from the bypass circuit, and a multiplexer configured to select between data from the first circuit and data from the second circuit are not inherent in Usami. As the Federal Circuit has stated, "[i]nherent anticipation requires that the missing descriptive material is 'necessarily present,' not merely probably or possibly present, in the prior art." *Trintec Indus., v. Top-U.S.A. Corp.*, 63 USPQ2d 1597, 1599 (Fed. Cir. 2002) (quoting *In re Robertson*, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)). Since serializing data in Usami could be performed without utilizing each of a first circuit, a second circuit, and a multiplexer as recited in claim 8, the limitations of claim 8 are not inherent in Usami as submitted by the Examiner.

Further, as indicated in the Manual of Patent Examining Procedure, "[o]fficial notice unsupported by documentary evidence should only be taken by the examiner where the facts asserted to be well-known, or to be common knowledge in the art are capable of instant and unquestionable demonstration as being well-known." M.P.E.P § 2144.03(A). "It would not be appropriate for the examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well-known." *Id.* (emphasis in original). Appellant contends that these limitations of claim 8 are not well known facts that are capable of instant

and unquestionable demonstration as being well known. Accordingly, Appellant submits that official notice is not appropriate is this case.

In view of the above, Appellant respectfully requests reversal of the rejection of claim 8 under 35 U.S.C. § 103(a).

IV. Rejection of claims 17 and 18 under 35 U.S.C. § 102(b) as being unpatentable over Usami and rejection of claims 19-24 under 35 U.S.C. § 103(a) as being unpatentable over Usami.

Independent claim 17 is patentably distinct from Usami.

Appellant submits that Usami fails to teach or suggest the invention recited by independent claim 17 including **a bypass circuit that bypasses the first in/first out memory; and a control circuit configured to provide first signals and second signals, wherein the first signals latch data from the first in/first out memory to provide a column address strobe latency of greater than one and the second signals latch data from the bypass circuit to provide a column address strobe latency of one.**

Usami discloses that each SDRAM includes a DRAM core 37. The DRAM core 37 is constructed from a plurality of banks. The SDRAM further includes a clock buffer 30, a command decoder 31, an address buffer/register and bank select 32, a pair of control signal latches 34, a mode register 35, a pair of column address counters 36, and an I/O data buffer/register 33. (Col. 7, line 64 - col. 8, line 3). The I/O data buffer/register 33 serves as a buffer circuit or register circuit for temporarily storing data to be written to the DRAM core 37 or for temporarily storing data read from the DRAM core 37. The I/O data buffer/register 33 is connected to the corresponding data bus "I/O data DQ0-DQ3" that is connected to the CPU 1. (Col. 9, lines 62 - col. 10, line 1).

The Examiner submits "SDRAM is inherently created from a memory array, a memory configured to receive data from the array, a bypass circuit, and a circuit that will select the programmed mode. Figure 4 shows that depending on the contents of the CAS Latency bits A4, A5, and A6 the CL (CAS latency) will vary accordingly as described in Claims 2 and 3." (Final Office Action mailed September 20, 2006, page 3). The Examiner also submits in the Response to Arguments "Usami teaches varying CAS Latencies (CLs). Cache Latencies are varied by changing the number of pipeline stages in the cache. A CL of

one means that a cache has one pipeline stage, a CL of two means two pipeline stages, and so on. Therefore, in providing multiple CLs Usami inherently teaches bypassing one or more pipeline stages based on setting of the CAS Latency bits. In bypassing a pipeline stage, a bypass circuit and a circuit configured to select between receiving data are inherent." (Final Office Action mailed September 20, 2006, pages 5-6).

Appellant submits that it is not inherent in Usami that a bypass circuit is used as recited in claim 17. As the Federal Circuit has stated, "[i]nherent anticipation requires that the missing descriptive material is 'necessarily present,' not merely probably or possibly present, in the prior art." *Trintec Indus., v. Top-U.S.A. Corp.*, 63 USPQ2d 1597, 1599 (Fed. Cir. 2002) (quoting *In re Robertson*, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)). Since varying the CAS latency in Usami could be performed without utilizing a bypass circuit as recited in claim 17, the limitations of claim 17 are not inherent in Usami as submitted by the Examiner. In addition, there is not a single reference to a cache memory including pipeline stages in Usami.

Figures 2 and 4 and the associated text of Usami do not disclose a bypass circuit or a control circuit configured to provide first signals and second signals, wherein the first signals latch data from the first in/first out memory to provide a column address strobe latency of greater than one and the second signals latch data from the bypass circuit to provide a column address strobe latency of one as recited in independent claim 17. In contrast, Usami merely discloses an I/O data buffer/register 33 for receiving data from the DRAM core 37 or writing data to the DRAM core 37. Nowhere in the text or figures does Usami disclose a bypass circuit for routing the data around I/O data buffer/register 33 based on a column address strobe latency. There is also no teaching or suggestion that I/O data buffer/register 33 includes pipeline stages. Even if I/O data buffer/register 33 did include pipeline stages, I/O data buffer/register 33 does not receive first and second signals from a control circuit for selecting a pipeline stage.

The mode register 35 is for extracting operation mode information, such as the CAS latency, the burst type, and the burst length, from the address data A0-A11 when the mode register 35 receives the address data A0-A11 in correspondence with a predetermined "mode register set" command that is received from the command decoder 31. Mode register 35 supplies each column address counter 36 with a control signal designating the burst length,

the burst type, and the CAS latency, thereby controlling count up timing and count up number of the column address counter 36. (Col. 9, lines 45-62). Therefore, Usami discloses controlling the CAS latency based on controlling the column address counter 36, not by using a bypass circuit as recited in claim 17.

In view of the above, Appellant respectfully requests reversal of the rejection of independent claim 17 under 35 U.S.C. § 102(b). Dependent claims 18-24 further define patentably distinct independent claim 17. Accordingly, Appellant believes these dependent claims are also allowable over the cited reference. Appellant respectfully requests reversal of the rejection of claim 18 under 35 U.S.C. § 102(b) and the rejection of claims 19-24 under 35 U.S.C. § 103(a).

V. Rejection of claims 25-30 under 35 U.S.C. § 103(a) as being unpatentable over Usami.

Usami fails to render independent claim 25 *prima facie* obvious.

Appellant submits that Usami fails to teach or suggest the invention recited by independent claim 25 including **a bypass circuit configured to bypass the memory circuit; a first rise/fall circuit configured to receive data from the memory circuit to provide a first output signal; a second rise/fall circuit configured to receive data from the bypass circuit to provide a second output signal; and a multiplexer configured to select between the first output signal and the second output signal based on a column address strobe latency select signal.**

Usami discloses that each SDRAM includes a DRAM core 37. The DRAM core 37 is constructed from a plurality of banks. The SDRAM further includes a clock buffer 30, a command decoder 31, an address buffer/register and bank select 32, a pair of control signal latches 34, a mode register 35, a pair of column address counters 36, and an I/O data buffer/register 33. (Col. 7, line 64 - col. 8, line 3). The I/O data buffer/register 33 serves as a buffer circuit or register circuit for temporarily storing data to be written to the DRAM core 37 or for temporarily storing data read from the DRAM core 37. The I/O data buffer/register 33 is connected to the corresponding data bus "I/O data DQ0-DQ3" that is connected to the CPU 1. (Col. 9, lines 62 - col. 10, line 1).

The Examiner submits "SDRAM is inherently created from a memory array, a memory configured to receive data from the array, a bypass circuit, and a circuit that will select the programmed mode." (Final Office Action mailed September 20, 2006, page 3). The Examiner also submits in the Response to Arguments "Usami teaches varying CAS Latencies (CLs). Cache Latencies are varied by changing the number of pipeline stages in the cache. A CL of one means that a cache has one pipeline stage, a CL of two means two pipeline stages, and so on. Therefore, in providing multiple CLs Usami inherently teaches bypassing one or more pipeline stages based on setting of the CAS Latency bits. In bypassing a pipeline stage, a bypass circuit and a circuit configured to select between receiving data are inherent." (Final Office Action mailed September 20, 2006, pages 5-6).

Appellant submits that it is not inherent in Usami that a bypass circuit is used as recited in claim 25. As the Federal Circuit has stated, "[i]nherent anticipation requires that the missing descriptive material is 'necessarily present,' not merely probably or possibly present, in the prior art." *Trintec Indus., v. Top-U.S.A. Corp.*, 63 USPQ2d 1597, 1599 (Fed. Cir. 2002) (quoting *In re Robertson*, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)). Since varying the CAS latency in Usami could be performed without utilizing a bypass circuit as recited in claim 25, the limitations of claim 25 are not inherent in Usami as submitted by the Examiner. In addition, there is not a single reference to a cache memory including pipeline stages in Usami.

Figures 2 and 4 and the associated text of Usami do not disclose a bypass circuit. In contrast, Usami merely discloses an I/O data buffer/register 33 for receiving data from the DRAM core 37 or writing data to the DRAM core 37. Nowhere in the text or figures does Usami disclose a bypass circuit for routing the data around I/O data buffer/register 33 based on a column address strobe latency select signal. There is also no teaching or suggestion that I/O data buffer/register 33 includes pipeline stages. Even if I/O data buffer/register 33 did include pipeline stages, I/O data buffer/register 33 does not receive a CAS latency select signal for selecting a pipeline stage. The CAS latency select signal is only provided to column address counter 36.

The mode register 35 is for extracting operation mode information, such as the CAS latency, the burst type, and the burst length, from the address data A0-A11 when the mode register 35 receives the address data A0-A11 in correspondence with a predetermined "mode

register set" command that is received from the command decoder 31. Mode register 35 supplies each column address counter 36 with a control signal designating the burst length, the burst type, and the CAS latency, thereby controlling count up timing and count up number of the column address counter 36. (Col. 9, lines 45-62). Therefore, Usami discloses controlling the CAS latency based on controlling the column address counter 36, not by using a bypass circuit as recited in claim 25.

Further, there is no teaching or suggestion in Usami of a first rise/fall circuit configured to receive data from the bypass circuit to provide a first output signal and a second rise/fall circuit configured to receive data from the bypass circuit to provide a second output signal. In addition, there is no teaching or suggestion in Usami of a multiplexer, let alone a multiplexer configured to select between the first output signal and the second output signal based on the CAS latency select signal. In contrast, Usami discloses a single circuit, I/O data buffer register 33, for temporarily storing data to be written to the DRAM core 37 or for temporarily storing data read from the DRAM core 37. (Col. 9, lines 63-66). Regarding these limitations, the Examiner states:

> A programmable SDRAM must inherently contain circuit means for serializing data as initiated by an edge of a clock cycle. The Examiner takes official notice that any combination of clock edges can be combined to provide the instruction to receive data. The motivation for doing so would be to increase system speed for read and write commands. Therefore it would be obvious to use any combination of clock edges to provide the instruction to receive data so that the system can be configured to increase system speed for read and write commands to obtain the invention claimed. (Final Office Action mailed September 20, 2006, page 4).

Usami, however, fails to teach or suggest these claim limitations. In Addition, Appellant submits that a first rise/fall circuit configured to receive data from the memory to provide a first output signal, a second rise/fall circuit configured to receive data from the bypass circuit to provide a second output signal, and a multiplexer configured to select between the first output signal and the second output signal are not inherent in Usami. As the Federal Circuit has stated, "[i]nherent anticipation requires that the missing descriptive material is 'necessarily present,' not merely probably or possibly present, in the prior art." *Trintec Indus., v. Top-U.S.A. Corp.*, 63 USPQ2d 1597, 1599 (Fed. Cir. 2002) (quoting *In re*

Robertson, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)). Since serializing data in Usami could be performed without utilizing each of a first rise/fall circuit, a second rise/fall circuit, and a multiplexer as recited in claim 25, the limitations of claim 25 are not inherent in Usami as submitted by the Examiner.

Further, as indicated in the Manual of Patent Examining Procedure, "[o]fficial notice unsupported by documentary evidence should only be taken by the examiner where the facts asserted to be well-known, or to be common knowledge in the art are capable of instant and unquestionable demonstration as being well-known." M.P.E.P § 2144.03(A). "It would not be appropriate for the examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well-known." *Id.* (emphasis in original). Appellant contends that these limitations of claim 25 are not well known facts that are capable of instant and unquestionable demonstration as being well known. Accordingly, Appellant submits that official notice is not appropriate is this case.

In view of the above, Appellant respectfully requests reversal of the rejection of claim 25 under 35 U.S.C. § 103(a). Dependent claims 26-30 further define patentably distinct independent claim 25. Accordingly, Appellant believes these dependent claims are also allowable over the cited reference. Appellant respectfully requests reversal of the rejection of claims 26-30 under 35 U.S.C. § 103(a).

VI. Rejection of claims 34-38 under 35 U.S.C. § 103(a) as being unpatentable over Usami.

Usami fails to render independent claim 34 *prima facie* obvious.

Appellant submits that Usami fails to teach or suggest the invention recited by independent claim 34 including **receiving data read from the array of memory cells in a bypass circuit during the clock cycle; and retrieving the data from the bypass circuit during the clock cycle.**

Usami discloses that each SDRAM includes a DRAM core 37. The DRAM core 37 is constructed from a plurality of banks. The SDRAM further includes a clock buffer 30, a command decoder 31, an address buffer/register and bank select 32, a pair of control signal latches 34, a mode register 35, a pair of column address counters 36, and an I/O data

buffer/register 33. (Col. 7, line 64 - col. 8, line 3). The I/O data buffer/register 33 serves as a buffer circuit or register circuit for temporarily storing data to be written to the DRAM core 37 or for temporarily storing data read from the DRAM core 37. The I/O data buffer/register 33 is connected to the corresponding data bus "I/O data DQ0-DQ3" that is connected to the CPU 1. (Col. 9, lines 62 - col. 10, line 1).

The Examiner submits "SDRAM is inherently created from a memory array, a memory configured to receive data from the array, a bypass circuit, and a circuit that will select the programmed mode." (Final Office Action mailed September 20, 2006, page 3). The Examiner also submits in the Response to Arguments "Usami teaches varying CAS Latencies (CLs). Cache Latencies are varied by changing the number of pipeline stages in the cache. A CL of one means that a cache has one pipeline stage, a CL of two means two pipeline stages, and so on. Therefore, in providing multiple CLs Usami inherently teaches bypassing one or more pipeline stages based on setting of the CAS Latency bits. In bypassing a pipeline stage, a bypass circuit and a circuit configured to select between receiving data are inherent." (Final Office Action mailed September 20, 2006, pages 5-6).

Appellant submits that it is not inherent in Usami that a bypass circuit is used as recited in claim 34. As the Federal Circuit has stated, "[i]nherent anticipation requires that the missing descriptive material is 'necessarily present,' not merely probably or possibly present, in the prior art." *Trintec Indus., v. Top-U.S.A. Corp.*, 63 USPQ2d 1597, 1599 (Fed. Cir. 2002) (quoting *In re Robertson*, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)). Since providing a CAS latency of one in Usami could be performed without utilizing a bypass circuit as recited in claim 34, the limitations of claim 34 are not inherent in Usami as submitted by the Examiner. In addition, there is not a single reference to a cache memory including pipeline stages in Usami.

Figures 2 and 4 and the associated text of Usami do not disclose receiving data read from the array of memory cells in a bypass circuit during the clock cycle or receiving the data from the bypass circuit during the clock cycle as recited in independent claim 34. In contrast, Usami merely discloses an I/O data buffer/register 33 for receiving data from the DRAM core 37 or writing data to the DRAM core 37. Nowhere in the text or figures does Usami disclose a bypass circuit for routing the data around I/O data buffer/register 33 based on a column

address strobe latency of one. There is also no teaching or suggestion that I/O data buffer/register 33 includes pipeline stages.

The mode register 35 is for extracting operation mode information, such as the CAS latency, the burst type, and the burst length, from the address data A0-A11 when the mode register 35 receives the address data A0-A11 in correspondence with a predetermined "mode register set" command that is received from the command decoder 31. Mode register 35 supplies each column address counter 36 with a control signal designating the burst length, the burst type, and the CAS latency, thereby controlling count up timing and count up number of the column address counter 36. (Col. 9, lines 45-62). Therefore, Usami discloses controlling the CAS latency based on controlling the column address counter 36, not by using a bypass circuit as recited in claim 34.

Further, there is no teaching or suggestion in Usami of receiving the data from the bypass circuit during the clock cycle that initiated the read command. In contrast, Usami discloses a single circuit, I/O data buffer register 33, for temporarily storing data to be written to the DRAM core 37 or for temporarily storing data read from the DRAM core 37. (Col. 9, lines 63-66). Regarding these limitations, the Examiner states:

> A programmable SDRAM must inherently contain circuit means for serializing data as initiated by an edge of a clock cycle. The Examiner takes official notice that any combination of clock edges can be combined to provide the instruction to receive data. The motivation for doing so would be to increase system speed for read and write commands. Therefore it would be obvious to use any combination of clock edges to provide the instruction to receive data so that the system can be configured to increase system speed for read and write commands to obtain the invention claimed. (Final Office Action mailed September 20, 2006, page 4).

Usami, however, fails to teach or suggest these claim limitations. In Addition, Appellant submits that retrieving the data from a bypass circuit during the clock cycle that initiated a read command is not inherent in Usami. As the Federal Circuit has stated, "[i]nherent anticipation requires that the missing descriptive material is 'necessarily present,' not merely probably or possibly present, in the prior art." *Trintec Indus., v. Top-U.S.A. Corp.*, 63 USPQ2d 1597, 1599 (Fed. Cir. 2002) (quoting *In re Robertson*, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)). Since a CAS latency of one in Usami could be provided without

retrieving the data from a bypass circuit during the clock cycle as recited in claim 34, the limitations of claim 34 are not inherent in Usami as submitted by the Examiner.

Further, as indicated in the Manual of Patent Examining Procedure, "[o]fficial notice unsupported by documentary evidence should only be taken by the examiner where the facts asserted to be well-known, or to be common knowledge in the art are capable of instant and unquestionable demonstration as being well-known." M.P.E.P § 2144.03(A). "It would not be appropriate for the examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well-known." *Id.* (emphasis in original). Appellant contends that these limitations of claim 34 are not well known facts that are capable of instant and unquestionable demonstration as being well known. Accordingly, Appellant submits that official notice is not appropriate is this case.

In view of the above, Appellant respectfully requests reversal of the rejection of claim 34 under 35 U.S.C. § 103(a). Dependent claims 35-38 further define patentably distinct independent claim 34. Accordingly, Appellant believes these dependent claims are also allowable over the cited reference. Appellant respectfully requests reversal of the rejection of claims 35-38 under 35 U.S.C. § 103(a).

RECEIVED
CENTRAL FAX CENTER

FEB 2 0 2007

CONCLUSION

For the above reasons, Appellant respectfully submits that the cited reference neither anticipates nor renders obvious claims of the pending Application. The pending claims distinguish over the cited reference, and therefore Appellant respectfully submits that the rejections must be withdrawn, and respectfully request the Examiner be reversed and claims 1-38 be allowed.

Any inquiry regarding this Appeal Brief should be directed to Mark A. Peterson at Telephone No. (612) 573-0120, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

Dicke, Billig & Czaja
Fifth Street Towers, Suite 2250
100 South Fifth Street
Minneapolis, MN 55402

Respectfully submitted,

Torsten Partsch,

By his attorneys,

DICKE, BILLIG & CZAJA, PLLC
Fifth Street Towers, Suite 2250
100 South Fifth Street
Minneapolis, MN 55402
Telephone: (612) 573-0120
Facsimile: (612) 573-2005

Dated: 2/20/2007
MAP:kmh

Mark A. Peterson
Reg. No. 50,485

CERTIFICATE UNDER 37 C.F.R. 1.8:

The undersigned hereby certifies that this paper or papers, as described herein, are being transmitted via facsimile to Facsimile No. (571) 273-8300 on this 20th day of February, 2007.

By: _____
Name: Mark A. Peterson

RECEIVED
CENTRAL FAX CENTER

FEB 2 0 2007

CLAIMS APPENDIX

1. (Previously Presented) A random access memory, comprising:

an array of memory cells;

a memory configured to receive data from the array of memory cells;

a bypass circuit configured to receive the data from the array of memory cells and to bypass the memory; and

a circuit configured to select between receiving the data from the memory to provide first output signals and receiving the data from the bypass circuit to provide second output signals based on a column address strobe latency select signal.

2. (Previously Presented) The random access memory of claim 1, wherein the circuit is configured to receive the data from the bypass circuit and provide the second output signals if the column address strobe latency select signal indicates a column address strobe latency value of one.

3. (Previously Presented) The random access memory of claim 1, wherein the circuit is configured to receive the data from the memory and provide the first output signals if the column address strobe latency select signal indicates a column address strobe latency value of greater than one.

4. (Original) The random access memory of claim 1, wherein the circuit comprises a first circuit configured to receive first rise and fall signals to serialize the data from the memory.

5. (Original) The random access memory of claim 4, wherein the circuit is configured to provide the first rise and fall signals after a first clock cycle is completed following a read command that is initiated by a first edge of the first clock cycle.

6. (Original) The random access memory of claim 4, wherein the circuit comprises a second circuit configured to receive second rise and fall signals to serialize the data from the bypass circuit.

7. (Original) The random access memory of claim 6, wherein the circuit is configured to provide the first rise and fall signals after a first clock cycle is completed following a read command that is initiated by a first edge of the first clock cycle and the second rise and fall signals during the first clock cycle.

8. (Previously Presented) The random access memory of claim 6, wherein the circuit comprises a multiplexer configured to select between serialized data from the first circuit and serialized data from the second circuit based on the column address strobe latency select signal.

9. (Original) The random access memory of claim 1, wherein the circuit comprises a rise and fall circuit configured to receive first rise and fall signals to serialize the data from the memory and to receive second rise and fall signals to serialize the data from the bypass circuit.

10. (Previously Presented) The random access memory of claim 9, wherein the circuit is configured to select between providing the first rise and fall signals and providing the second rise and fall signals based on the column address strobe latency select signal.

11. (Original) The random access memory of claim 10, wherein the circuit is configured to provide the first rise and fall signals after a first clock cycle is completed following a read command that is initiated by a first edge of the first clock cycle and the second rise and fall signals during the first clock cycle.

12. (Previously Presented) The random access memory of claim 1, wherein the bypass circuit is configured to tri-state an output if the column address strobe latency select signal indicates a column address strobe latency value of greater than one.

13. (Original) The random access memory of claim 1, wherein the memory comprises a first in/first out memory.

14. (Original) The random access memory of claim 1, wherein the random access memory is a low power synchronous dynamic random access memory.

15. (Original) The random access memory of claim 1, wherein the random access memory is a double data rate-I synchronous dynamic random access memory.

16. (Original) The random access memory of claim 1, wherein the random access memory is a double data rate-II synchronous dynamic random access memory.

17. (Original) A random access memory, comprising:

a first in/first out memory;

a bypass circuit that bypasses the first in/first out memory; and

a control circuit configured to provide first signals and second signals, wherein the first signals latch data from the first in/first out memory to provide a column address strobe latency of greater than one and the second signals latch data from the bypass circuit to provide a column address strobe latency of one.

18. (Previously Presented) The random access memory of claim 17, wherein the control circuit comprises a clock signal multiplexer configured to select between providing the first signals and the second signals based on a column address strobe latency select signal.

19. (Original) The random access memory of claim 17, comprising a rise/fall circuit configured to receive the first signals and the second signals to provide one data bit at a time.

20. (Original) The random access memory of claim 19, wherein the control circuit is configured to provide the first signals comprising a first rise signal and a first fall signal that is the inverse of the first rise signal and the second signals comprising a second rise signal and a second fall signal that is the inverse of the second rise signal.

21. (Original) The random access memory of claim 20, wherein the rise/fall circuit is configured to provide a first data bit as output on a rising edge of the first rise signal and a second data bit as output on a rising edge of the first fall signal.

22. (Original) The random access memory of claim 19, comprising a data delay circuit electrically coupled to the rise/fall circuit and configured to adjust output timing of the data.

23. (Original) The random access memory of claim 22, comprising an off chip driver configured to pass data from the data delay circuit to a data pad.

24. (Original) The random access memory of claim 17, wherein the bypass comprises a tri-state output that is set to a high impedance state for the column address strobe latency of greater than one.

25. (Previously Presented) A random access memory, comprising:

a memory circuit;

a bypass circuit configured to bypass the memory circuit;

a first rise/fall circuit configured to receive data from the memory circuit to provide a first output signal;

a second rise/fall circuit configured to receive data from the bypass circuit to provide a second output signal; and

a multiplexer configured to select between the first output signal and the second output signal based on a column address strobe latency select signal.

26. (Previously Presented) The random access memory of claim 25, wherein the multiplexer selects the first output signal if the column address strobe latency signal indicates the column address strobe latency is greater than one and the second output signal if the column address strobe latency select signal indicates the column address strobe latency is one.

27. (Original) The random access memory of claim 25, comprising a controller configured to provide a first signal and a second signal to the first rise/fall circuit and a third signal and a fourth signal to the second rise/fall circuit.

28. (Original) The random access memory of claim 27, wherein the controller is configured to create the first signal and the second signal from a clock signal and the third signal and the fourth signal from the inverted clock signal.

29. (Original) The random access memory of claim 28, wherein the first rise/fall circuit outputs a first data bit on a rising edge of the first signal and a second data bit on a rising edge of the second signal.

30. (Original) The random access memory of claim 28, wherein the second rise/fall circuit outputs a first data bit on a rising edge of the third signal and a second data bit on a rising edge of the fourth signal.

31. (Original) A random access memory comprising:

means for storing data read from an array of memory cells;

means for receiving the data read from the array of memory cells to bypass the means for storing data;

means for retrieving the data from the means for storing the data if column address strobe latency is greater than one;

means for retrieving the data from the means for receiving the data if the column address strobe latency is one.

32. (Original) The random access memory of claim 31, wherein the means for storing data comprises a first in/first out memory.

33. (Original) The random access memory of claim 31, comprising means for serializing the data retrieved from the means for storing and the means for receiving to provide serial data bit output signals.

34. (Original) A method for reading data from a random access memory in a column address strobe latency of one, comprising:

initiating a read command on a first edge of a clock cycle;

receiving data read from the array of memory cells in a bypass circuit during the clock cycle; and

retrieving the data from the bypass circuit during the clock cycle.

35. (Original) The method of claim 34, comprising bypassing first in/first out memory cells used to provide data if the column address strobe latency is greater than one.

36. (Original) The method of claim 34, comprising:

generating an inverted clock signal from a data clock signal to retrieve the data from the bypass circuit.

37. (Original) The method of claim 36, comprising:

generating a first signal and a second signal from the inverted clock signal to retrieve the data from the bypass circuit.

38. (Original) The method of claim 37, comprising outputting a first data bit on a rising edge of the first signal and a second data bit on a rising edge of the second signal.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.